APPARATUS FOR CONTROLLING A BOOSTED VOLTAGE AND METHOD OF CONTROLLING A BOOSTED VOLTAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application relies for priority upon Korean Patent Application No. 2003-55744 filed on August 12, 2003, the contents of which are herein incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to an apparatus for controlling a boosted voltage and a method of controlling the boosted voltage.

2. Description of the Related Art

[0003] Portable electric devices are provided with a portable power supply such as a battery. The portable power supply usually has a voltage source lower than 3 volts.

[0004] Electric devices coupled to the portable electric devices operate using a high voltage source, and thus require a device for boosting the voltage of the portable power supply to a fixed driving voltage.

[0005] U.S. Patents 6,534,963 and 6,445,623 both disclose conventional apparatuses for boosting voltage. However, the boosted voltages produced by these apparatuses have a large ripple voltage when a large load current flows through the load.

SUMMARY OF THE INVENTION

In the method of controlling a boosted voltage according to the present

invention, a boosted voltage is produced from an input voltage based on a control current, and the control current is generated based on the boosted voltage.

In an exemplary embodiment of the apparatus for controlling a boosted voltage according to the present invention, a voltage generating circuit is configured to generate the boosted voltage from the input voltage based on the control current; and a control circuit is configured to generate the control current based on the boosted voltage. The method and apparatus provide a stable voltage level for the boosted voltage, which has reduced ripple.

In one exemplary embodiment, the voltage generating circuit includes first, second, third and fourth switches. A capacitor stores charges corresponding to the input voltage while the first and third switches are turned on, and outputs the boosted voltage while the second and fourth switches are turned on. In this embodiment, a clock signal generator is configured to generate first, second and third clock signals, and a level shifter circuit is configured to selectively change a level of the input voltage in response to the third clock signal to output a switching control signal. The first and second switches are switched in response to first and second clock signals, and the third and fourth switches are switched in response to a switch control signal.

In an exemplary embodiment, the third clock signal has an inverted phase with respect to the first clock signal, a front edge of the second clock signal is delayed by a fixed time with respect to a front edge of the first clock signal, and an active period of the second clock signal is narrower than that of the first clock signal.

In another exemplary embodiment, the control circuit is configured to generate the control current based on the boosted voltage and a desired boosted voltage. For example, the control circuit is configured to generate the control current

based on a difference between the boosted voltage and the desired boosted voltage.

In an exemplary embodiment, the control circuit includes a voltage divider configured to divide the boosted voltage to generate a divided voltage and an amplifier configured to amplify a voltage difference between a reference voltage and the divided voltage. For example, the reference voltage represents a desired boosted voltage. A voltage controlled current source in the control circuit is configured to generate the control current based on the amplified difference voltage

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The above and other advantages of the present invention will become more apparent by describing in detail the exemplary embodiments thereof with reference to the accompanying drawings, in which:

[0007] FIG. 1 is a block diagram showing an apparatus for controlling a boosted voltage according to one exemplary embodiment of the present invention;

[0008] FIG. 2 is an exemplary circuit level diagram of the apparatus illustrated in FIG. 1;

[0009] FIG. 3 is a timing diagram showing clock signals of FIG. 1;

[0010] FIG. 4 is a graph showing an output voltage of the apparatus of FIG.1, an output voltage of a differential amplifier of FIG. 1, and an output of a voltage divider of FIG. 1;

[0011] FIG. 5 is a graph showing the output voltage of the apparatus of FIG. 1 and the output voltage of the differential amplifier of FIG. 1 as a load current varies; and

[0012] FIG. 6 is a flow chart showing a method of controlling the boosted voltage.

DESCRIPTION OF EMBODIMENTS

[0013] Hereinafter the exemplary embodiment of the present invention will be described in detail with reference to the accompanying drawings.

[0014] FIG. 1 is a block diagram showing an apparatus for controlling a boosted voltage according to one exemplary embodiment of the present invention, and FIG. 2 is an exemplary circuit level diagram of the apparatus shown in FIG. 1.

[0015] Referring to FIGS. 1 and 2, the apparatus for controlling the boosted voltage includes a clock signal generator 200, a level shifter 210, first and second switches S1 and S2, third and fourth switches S3 and S4 and a capacitor Cpump forming a voltage generating circuit generating a boosted voltage (Vout) from an input voltage (V_{DD}) based on a control current (Ictrl). The apparatus further includes a reference signal generator 220, a voltage divider 230, an amplifier 240, and a voltage controlled current source (VCCS) 250 forming a control circuit generating the control current Ictrl.

[0016] The clock signal generator 200 generates first, second and third clock signals (clock1, clock2, clcok3). The level shifter 210 changes a level of the input voltage V_{DD} in response to the first clock signal clock1 to generate a switching control signal . The reference signal generator 220 generates a reference voltage (Vref) representing the desired boosted voltage. The voltage divider 230 divides boosted voltage Vout to generate a divided voltage (Vd) representing the boosted voltage Vout. The amplifier 240 amplifies a difference voltage between the reference voltage Vref and the divided voltage Vd to generate a control voltage (Vctrl). The voltage controlled current source 250 generates the control current Ictrl based on the control voltage Vctrl. The apparatus for controlling the boosted voltage

is connected to a load 260 such as a capacitor C and a resistor R connected in parallel to the capacitor C. The boosted voltage Vout is provided to the load 260.

[0017] Referring to Fig. 2, the level shifter 210 includes first and second NMOS transistors (MN1, MN2) and a NMOS capacitor (MC). A first current electrode of the first NMOS transistor MN1 receives the input voltage V_{DD}, a control or gate electrode of the first NMOS transistor MN1 is connected to the first current electrode of the first NMOS transistor MN1, and a second current electrode of the first NMOS transistor MN1 is connected to the third switch S3. A first current electrode of the second NMOS transistor MN2 receives the input voltage V_{DD}, a second current electrode of the second NMOS transistor MN2 is connected to the second current electrode of the first NMOS transistor MN1, and a control or gate electrode of the second NMOS transistor MN2 is connected to the fourth switch S4. A control electrode of the NMOS capacitor MC is connected to the second current electrodes of the first and second NMOS transistors MN1 and MN2.

[0018] The voltage divider 230, for example, includes serially connected first, second, third and fourth resistors R1, R2, R3 and R4, and generates the divided voltage Vd based on the resistances of the resistors R1, R2, R3 and R4. In one exemplary embodiment, the resistors R1, R2, R3 and R4 may have the same resistance R. In one exemplary embodiment, the input voltage V_{DD} is about 3 volts, the desired boosted voltage is 5 volts. In this embodiment, the voltage divider 230 produces a divided voltage Vd of about 1.2 volts, which is substantially the same as the reference voltage Vref, when the boosted voltage is 5 volts.

[0019] As shown in Fig. 3, in one exemplary embodiment , the amplifier 240 may be a differential amplifier. An inverting (-) terminal of the differential amplifier 240

receives the reference voltage Vref, and a non-inverting (+) terminal of the differential amplifier 240 receives the divided voltage Vd.

[0020] In the exemplary embodiment of Fig 3, the VCCS 250 includes a first PMOS transistor MP1. A control electrode of the first PMOS transistor MP1 receives the output voltage of the differential amplifier 240, a first current electrode of the first PMOS transistor MP1 receives the input voltage V_{DD}, and a second current electrode of the first PMOS transistor MP1 is connected to the first switch S1.

[0021] The first switch S1, for example, includes a second PMOS transistor MP2. A control electrode of the second PMOS transistor MP2 receives the first clock signal clock 1, a first current electrode of the second PMOS transistor MP2 is connected to the second current electrode of the first PMOS transistor MP1, and a second current electrode of the second PMOS transistor MP2 is connected to the second switch S2.

[0022] The second switch S2 includes, for example, a third NMOS transistor MN3. A control electrode of the third NMOS transistor MN3 receives the second clock signal clock2, a second current electrode of the third NMOS transistor MN3 is connected to the second current electrode of the second PMOS transistor MP2, and a first current electrode of the third NMOS transistor MN3 is connected to a reference potential such as ground.

[0023] The third switch S3 includes, for example, a fourth NMOS transistor MN4. A second current electrode of the fourth NMOS transistor MN4 receives the input voltage V_{DD}, a control electrode of the fourth NMOS transistor MN4 is connected to the second current electrodes of the first and second NMOS transistors MN2 and MN3, and a first current electrode of the fourth NMOS transistor MN4 is connected to the capacitor Cpump.

[0024] The fourth switch S4 includes, for example, a third PMOS transistor MP3. A control electrode of the third PMOS transistor MP3 is connected to the control electrode of the fourth NMOS transistor MN4, a first current electrode of the third PMOS transistor MP3 is connected to the control electrode of the second NMOS transistor MN2 and the first current electrode of the fourth NMOS transistor MN4, and a second current electrode of the third PMOS transistor MP3 delivers the output voltage Vout.

[0025] A first electrode of the capacitor Cpump is connected to the control electrode of the second NMOS transistor MN2 and the first current electrode of the fourth NMOS transistor MN4. A second electrode of the capacitor Cpump is connected to the second current electrodes of the second and third NMOS transistors MN2 and MN3.

[0026] Hereinafter, the operation of the apparatus for controlling the boosted voltage is described.

[0027] The clock signal generator 200 generates the first, second and third clock signals clock1, clock2, clock3. Fig. 3 illustrates an exemplary embodiment of the first, second and third clock signals clock1, clock2, clock3 generated by the clock signal generator 200. As shown , the first clock signal clock1 repeats a high level and a low level with a fixed period. A front edge of the second clock signal clock2 is delayed by a fixed time Δt with respect to a front edge of the first clock signal clock1, and the high level period of the second clock signal clock2 is shorter than that of the first clock signal clock 1 such that the high level of a pulse in the second clock signal clock2 ends before the high level of a corresponding pulse in the first clock signal clock1. The third clock signal clock3 is an inverse of the first clock signal clock1.

[0028] The level shifter 210, as shown in FIG. 2, receives an inverted version of the third clock signal clock3 from an inverter IV and changes the level of the input voltage V_{DD} to generate the switch control signal. The switch control signal swings between the level of the input voltage V_{DD} and substantially double ($2V_{DD}$) the level of the input voltage.

[0029] The second switch S2 is turned on when the second clock signal clock2 has an active status such as a high level, and the third switch S3 is turned on when the switch control signal has a high level (i.e., substantially $2V_{DD}$). Charges corresponding to the input voltage V_{DD} are charged in the capacitor Cpump when the second and third switches S2 and S3 are turned on because the second and third switches S2 and S3 connect the capacitor Cpump between the input voltage V_{DD} and ground.

[0030] The first switch S1 is turned on when the first clock signal clock1 has a non-active status such as a low level, and the fourth switch S4 is turned on when the switch control signal has a low level (i.e., V_{DD}). Accordingly, the fourth switch S4 is turned off while the third switch S3 is turned on, and the fourth switch S4 is turned on while the third switch S3 is turned off.

[0031] The output voltage Vout, corresponding to the charges charged in the capacitor Cpump, is supplied to the load 260 as the first and fourth switches S1 and S4 are turned on. The fourth switch S4 connect the capacitor Cpump to the load 260, and the first switch S1 connects the capacitor Cpump with the VCCS 250. The VCCS 250 supplies charges to the capacitor Cpump so that the boosted voltage Vout reaches and maintains a desired boosted voltage. The amount of charge supplied to the capacitor Cpump by the VCCS 250 is regulated by the differential

amplifier 240. Namely, the differential amplifier 240 regulates the control current Ictrl output by the VCCS 240. The differential amplifier 240 makes the first PMOS transistor MP1 of the VCCS 250 more or less conductive based on the comparison of the divided voltage Vd with the reference voltage Vref (i.e., based on a comparison of the generated boosted voltage to the desired boosted voltage). By controlling the output voltage Vout using a control current Ictrl derived based on the output voltage Vout, the output voltage Vout has the desired stable voltage level (e.g., 5 volts) without ripple.

[0032] FIG. 4 is a graph showing an output voltage of the apparatus of FIG. 1, an output voltage of a differential amplifier of FIG. 1, and an output of a voltage divider of FIG. 1. Referring to FIG. 4, graph (a) shows variation of the output voltage Vout over time, graph (b) shows variation of the output voltage of the differential amplifier 240 over time, and graph (c) shows variation of the divided voltage Vd over time. In the example of Fig. 4, the desired voltage level for the output voltage is 5 volts .

[0033] As shown, the output voltage Vout gradually increases to the desired voltage level of 5 volts and is maintained at 5 volts. The output voltage of the differential amplifier 240 has a minimum voltage level until the output voltage of the differential amplifier 240 reaches 5 volts, and then a regulation operation occurs after the output voltage of the differential amplifier 240 reaches 5 volts.

[0034] The voltage divider 230 divides the boosted voltage Vout, and outputs 1.2 volts, which is substantially the same as the reference voltage Vref, of divided voltage Vd when the output voltage Vout reaches the desired voltage level of 5 volts. In one exemplary embodiment, the reference voltage generator 220 generates a constant reference voltage Vref regardless of process voltage and process

temperature.

[0035] The differential amplifier 240 compares the reference voltage Vref and the divided voltage Vd, amplifies the difference voltage between the reference voltage Vref and the divided voltage Vd, and outputs the difference voltage, also referred to as the control voltage Vctrl. The control voltage Vctrl represents a difference between the generated boosted voltage Vout and the desired boosted voltage.

[0036] The differential amplifier 240 outputs a first difference voltage when the reference voltage Vref is higher than the divided voltage Vd, outputs a reference difference voltage when the reference voltage Vref is the same as the divided voltage Vd, and outputs a second difference voltage when the reference voltage Vref is lower than the divided voltage Vd. The first difference voltage is lower than the reference difference voltage, and the second difference voltage is higher than the reference difference voltage.

[0037] The divided voltage Vd becomes higher than the reference voltage Vref when the output voltage Vout becomes higher than the desired voltage level (e.g., , 5 volts). Thus, the differential amplifier 240 outputs a voltage having level that is higher than the reference difference voltage when the output voltage Vout is higher than the desired voltage level. The divided voltage Vd becomes lower than the reference voltage Vref when the output voltage Vout becomes lower than the desired voltage level (e.g., 5 volts). Thus, the differential amplifier 240 outputs a voltage having a level that is lower than the reference difference voltage when the output voltage Vout is lower than the desired voltage level of 5 volts. The level of the output voltage Vout varies depending upon the load current (I_{load}) that flows through the load 260, and the voltage output from the differential amplifier 240 varies depending upon the

output voltage Vout. Accordingly, the VCCS 250 compensates for the variation in the output voltage Vout.

[0038] FIG. 5 is a graph showing the output voltage of the apparatus of FIG.1 and the output voltage of the differential amplifier of FIG. 1 as the load current varies.

[0039] Referring to FIG. 5, graph (a) shows the output voltage Vout as the load current varies, and graph (b) shows the output voltage of the differential amplifier 240 as the load current varies.

[0040] As shown in graph (a) of FIG. 5, the variation of the output voltage Vout is very small when the load current I_{load} has a low level, 1 mA, and the variation of the output voltage Vout increases when the level of the load current I_{load} increases to, for example, 15 mA.

[0041] In addition, the difference between the reference voltage Vref and the divided voltage Vd increases as the load current I_{load} changes from 1 mA to 15 mA, and thus the amplitude of the output voltage of the differential amplifier 240 increases. Therefore, the control current Ictrl output from the VCCS 250 increases as the load current I_{load} increases.

[0042] The VCCS 250 outputs the control current Ictrl corresponding to the voltage output from the differential amplifier 240. The control current Ictrl regulates the quantity of the charges charged in the capacitor Cpump to maintain the level of the output voltage Vout, thus the output voltage Vout has a stable voltage level.

[0043] For example, the differential amplifier 240 outputs the first difference voltage lower than the reference difference voltage when the output voltage Vout is lower than the desired boosted voltage level (e.g., 5 volts). As a result, the control current Ictrl output from the VCCS 250 increases, and the quantity of the charges charged in

the capacitor Cpump increases. Therefore, the output voltage Vout increases up to the desired boosted voltage level.

[0044] However, the differential amplifier 240 outputs the second difference voltage higher than the reference difference voltage when the output voltage Vout is higher than the desired boosted voltage level of about 5 volts, the control current Ictrl output from the VCCS 250 then decreases, and the quantity of the charges charged in the capacitor Cpump decreases. Accordingly, the output voltage Vout decreases down to the desired boosted voltage level, and the desired level of the output voltage Vout may be maintained.

[0045] FIG. 6 is a flow chart showing a method of controlling the boosted voltage. As shown, the output voltage Vout having a fixed boosted voltage level is generated according to the switching operation of the switches S1, S2, S3 and S4, which are turned on/off in response to the clock signals clock1, clock2 and clock3 (step S700). Particularly, the second switch S2 is turned on in response to the second clock signal clock2, the third switch S3 is turned on in response to the third clock signal clock3, and the charges corresponding to the input voltage V_{DD} are charged in the capacitor Cpump. The first switch S1 is turned on in response to the first clock signal clock1, the fourth switch S4 is turned on in response to the switch control signal that is generated in response to the third clock signal clock3, and the output voltage Vout corresponding to the charges in the capacitor Cpump are provided to the load 260.

[0046] The voltage divider 230 divides the output voltage Vout (step S702), and the differential amplifier 240 compares the divided voltage Vd and the reference voltage Vref to generate the difference voltage therebetween (step S704).

[0047] The divided voltage Vd becomes higher than the reference voltage Vref when the output voltage Vout is higher than the desired voltage level (e.g., 5 volts). The divided voltage Vd becomes lower than the reference voltage Vref when the output voltage Vout is lower than the desired voltage level (e.g., 5 volts). Thus, the differential amplifier 240 outputs a voltage having a level that is lower than the reference difference voltage when the output voltage Vout is lower than the desired voltage level. The differential amplifier 240 outputs a voltage having a level that is higher than the reference difference voltage when the output voltage Vout is higher than the desired voltage level.

[0048] The level of the output voltage Vout varies depending upon the load current I_{load} that flows through the load 260, and thus the voltage output from the differential amplifier 240 varies depending upon the output voltage Vout.

[0049] The VCCS 250 generates the control current Ictrl corresponding to the voltage outputted from the differential amplifier 240. The control current Ictrl regulates the quantity of the charges charged in the capacitor Cpump, and thus the output voltage Vout is maintained at a desired voltage level with reduced ripple voltage (step S706).

[0050] The level of the output voltage Vout is controlled by means of the control current (step S708). Particularly, the quantity of the control current Ictrl is decreased when the output voltage Vout is higher than the desired boosted voltage level, and the quantity of the control current Ictrl is increased when the output voltage Vout is lower than the desired boosted voltage level, so that the level of the output voltage Vout may be maintained.

[0051] While the exemplary embodiments of the present invention and its

advantages have been described in detail, it should be understood that various changes, substitutions and alterations may be made herein without departing from the scope of the invention.